Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **1 N.CLR**
2. **1 D**
3. **1 CLK**
4. **1 N.PRE**
5. **1 Q**
6. **1 N.Q**
7. **GND**
8. **2 N.Q**
9. **2 Q**
10. **2 N.PRE**
11. **2 CLK**
12. **2 D**
13. **2 N.CLR**
14. **VCC**

**.054”**

**.056”**

**12**

**11**

**10**

**9**

**2**

**3**

**4**

**5**

**6 7 8**

**1 14 13**

**MASK**

**REF**

**HC74E**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .0035” X .0035”**

**Backside Potential: Floating (or connect to Vcc)**

**Mask Ref: HC74E**

**APPROVED BY: DK DIE SIZE .054” X .056” DATE: 2/21/23**

**MFG: TEXAS INSTRUMENTS THICKNESS .010” P/N: 54HC74**

**DG 10.1.2**

#### Rev B, 7/19/02